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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,404	12/06/2001	Koji Nii	027260-505	5384

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EXAMINER	
TRAN, TAN N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,404	NII ET AL.	
	Examiner	.Art Unit	
	TAN N TRAN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,13,14 and 17* is/are rejected.

7)☒ Claim(s) *5,9-12,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on 09/04/02. These drawings are approved.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-8, 13,14,17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Igarashi et al (6,299,314) in view of Applicant's prior art figure 31.

With regard to claims 1,17 Igarashi et al. disclose a gate electrode 3 formed on a substrate 1 through a gate insulating film 2 lying therebetween; first and second diffused layers formed opposite to each other across the portion of the substrate 1 existing under the gate electrode 3 and having a first conduction type, each having a second conduction type different from the first conduction type of the portion; a contact CL12 formed within a contact hole CH12 on the substrate 1. (Note attachment # 1 of Fig. 20 of Igarashi et al.).

Igarachi et al. does not disclose a wiring layer formed above the gate electrode, so that the contact formed within a contact hole between the wiring layer and the substrate electrically connects the wiring layer to the first diffused layer and the gate electrode.

However, Applicant' prior art discloses a wiring layer formed above the gate electrode 30, so that the contact formed within a contact hole 60 between the wiring layer and the substrate 10 connects the wiring layer to the first diffused layer 20 and the gate electrode 30. (Note Fig. 31 of Applicant' prior art).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Igarachi et al.'s device having a wiring layer formed above the gate electrode, so that the contact formed within a contact hole between the wiring layer and the substrate connects the wiring layer to the first diffused layer and the gate electrode such as taught by Applicant' prior art in order to connect the semiconductor device to other element or to the power supply.

With regard to claim 2, Igarashi et al. discloses the contact CL12 is connected also to the second diffused layer. (Note attachment #1 of Fig. 20 of Igarashi et al.).

With regard to claim 3, Igarashi et al. discloses a third diffused layer formed on the substrate 1; and an isolation area ST formed between the first and the third diffused layers, which separates the first and the third diffused layers each other; wherein the contact CL12 is connected further to the third diffused layer. (Note attachment # 2 of Fig. 20 of Igarashi et al.).

With regard to claim 4, Igarashi et al. disclose a gate electrode 3 formed on a substrate 1 through a gate insulating film 2 lying therebetween; a diffused layer formed on the substrate having first and second diffused portions formed opposite to each other across the portion of the substrate 1 existing under the gate electrode 3 and having a first conduction type, each having a second conduction type different from the first conduction type of the portion of the substrate and a third portion that connects the first portion to the second portion; a contact CL12 formed within a contact hole CH12 on the substrate 1, (Note attachment # 2 of Fig. 20 of Igarashi et al.).

Igarachi et al. does not disclose a wiring layer formed above the gate electrode, so that the contact formed within a contact hole between the wiring layer and the substrate connects the wiring layer to the diffused layer and the gate electrode.

However, Applicant' prior art discloses a wiring layer formed above the gate electrode 30, so that the contact formed within a contact hole 60 between the wiring layer and the substrate 10 connects the wiring layer to the diffused layer 20 and the gate electrode 30. (Note Fig. 31 of Applicant' prior art).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Igarachi et al.'s device having a wiring layer formed above the gate electrode, so that the contact formed within a contact hole between the wiring layer and the substrate, which connects the wiring layer to diffused layer and the gate electrode, such as taught by Applicant' prior art in order to connect the semiconductor device to other element or to the power supply.

With regard to claim 6, Igarashi et al. discloses another diffused layer formed on the substrate 1; and an isolation area ST formed between the first portion of the diffused layer and the another diffused layer, which separates the first portion of the diffused layer and the another diffused layer, wherein the contact is connected further to the another diffused layer. (Note attachment # 2 of Fig. 20 of Igarashi et al.).

With regard to claims 7, 8, 13, 14 Igarashi et al. does not disclose the gate 3 is a memory node of the SRAM cell or the memory node of a bistable trigger circuit. However, it would have been obvious to one of ordinary skill in the art to form the gate 3 of Igarashi et al. functions as a memory node, because it is conventional in the art to use one of the gate electrodes that functions as a memory node. Note Fig. 1 of Sunami is cited to support for the well known position.

Although Igarashi et al. and Applicant's prior art do not teach exact the type of the device as that claimed by Applicant, the type differences are considered obvious design choices and are not patentable unless unobvious or expected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note in re Leshin, 125 USPQ 416.

Claim Objections

3. Claim 12 is objected to because of the following informalities:

In claim 12, line 7, "s" should be deleted.

Allowable Subject Matter

4. Claims 5, 9-12, 15,16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 5 is allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as the contact is connected to the first portion and the second portion of the diffused layer as recited in claim 5, the film thickness of the gate insulating film is thinner than the one of the other gate insulating film as recited in claim 9, the relative dielectric constant of the gate insulating film is higher than the one of the another gate insulating film as recited in claim 10, the impurity concentrations of the first diffused layer and the second diffused layer are higher than the ones of the source and the drain areas as recited in claim 11, the impurity concentrations of the diffused layer are higher than the

impurity concentration of the source area and the drain area as recited in claim 12, the film thickness of the gate insulating film is thinner than the one of the other gate insulating film as recited in claim 15, and the relative dielectric constant of the gate insulating film is higher than the one of the other gate insulating film as recited in claim 16.

Response to Arguments

5. Applicant's arguments filed 9/04/02 have been fully considered but they are not persuasive.

It is argued, at pages 8,9 of the remarks, that "The prior art does not show, teach or suggest a contact connecting a wiring layer to a gate electrode". However, fig. 31 of Applicant's prior art does show the contact that is form in the contact hole 60 connects the wiring layer to the gate electrode 30, because the contact connects the wiring to a top of the gate electrode 30 and to the SiO_2 sidewall, so the contact electrically connects the wiring layer to the top portion of the gate electrode 30.

It is argued, at page 11 of the remarks, that "nothing in Igarashi et al show, teaches or suggests that the contact connects the wiring layer to a gate electrode in claims 1 and 4 and new claim 17". However, Applicant's claims 1, 4, 17 do not recite the contact electrically connects the wiring layer to the gate electrode. Moreover, In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually

where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Thus, Igarashi et al. does not show the contact connects the wiring layer to the gate electrode, but applicant's prior art fig. 31 does show that the contact connects the wiring layer to the top portion of the gate electrode 30.

It is argued, at page 12 of the remarks, that "nothing in the combination shows, teaches or suggests that the contact which connects the wiring layer to a gate electrode in claims 1 and 4". However, Applicant's claims 1,4 do not distinguish over Igarashi et al. in view of Applicant's prior art fig. 31 because Applicant's claims 1, 4 do not recite the contact electrically connects the wiring layer to the gate electrode. Moreover, In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Thus, Igarashi et al. does not show the contact connects the wiring layer to the gate electrode, but applicant's prior art fig. 31 does show that the contact connects the wiring layer to the top portion of the gate electrode 30. Thus, Applicant's claims 1,4,7 do not distinguish over Igarashi and Applicant's prior art references.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

Oct 2002

Minh Loan Tran
Primary Examiner

Attachment # 1

FIG. 20

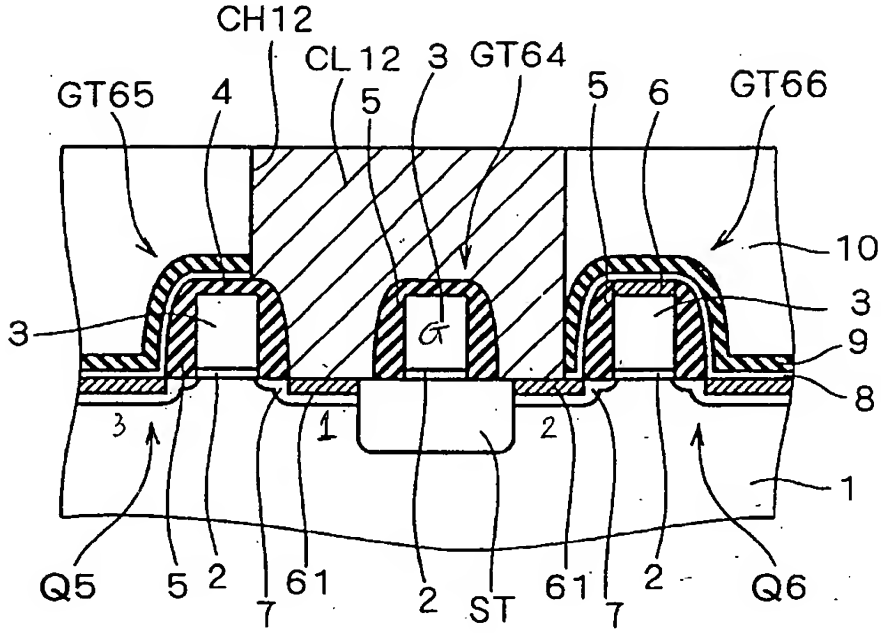
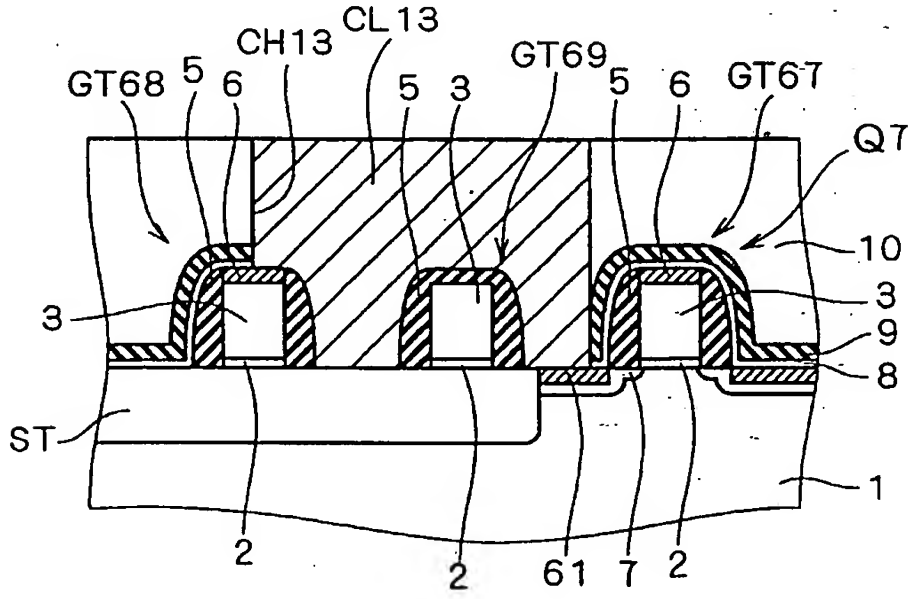


FIG. 21



Attachment # 2

FIG. 20

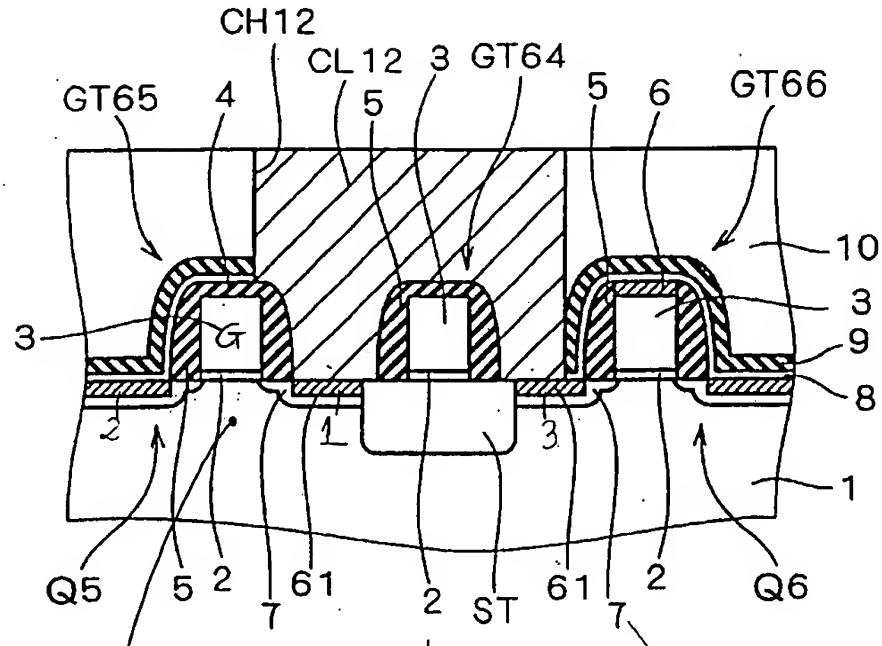
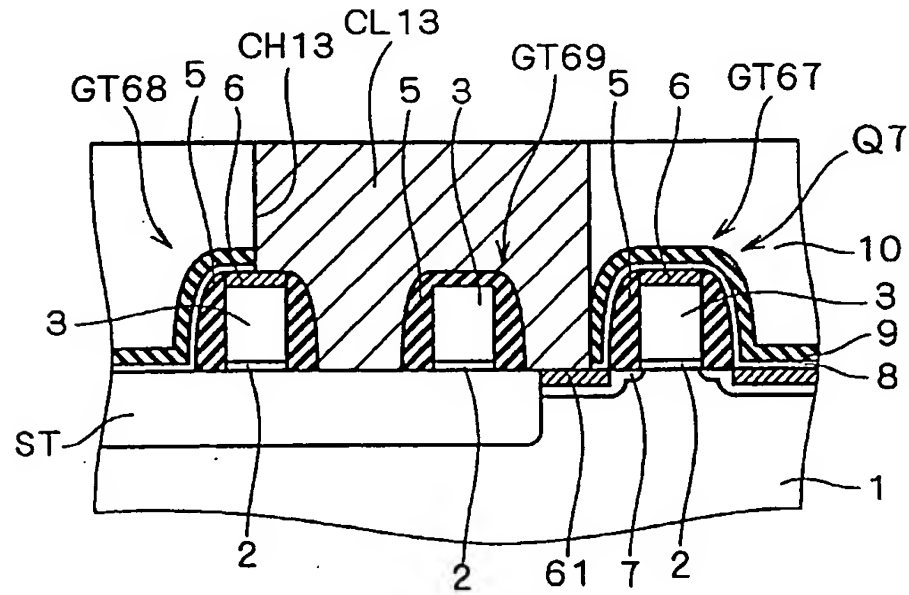


FIG. 21



Attachment # 2